

1-KBIT SERIAL ELECTRICALLY ERASABLE PROM

ADVANCED INFORMATION
NOVEMBER 2005

FEATURES

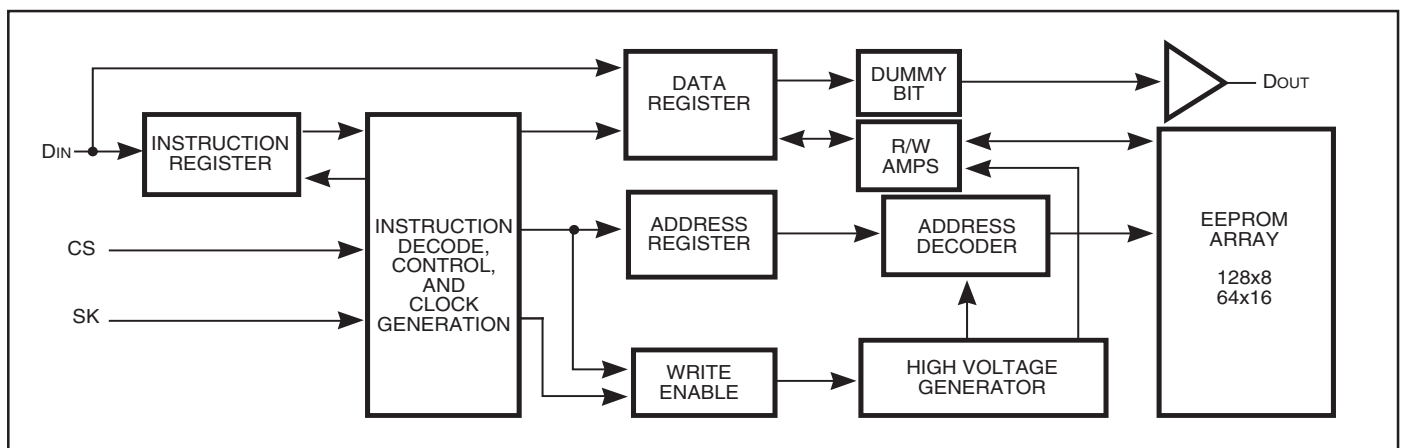
- Industry-standard Microwire Interface
 - Non-volatile data storage
 - Wide voltage operation:
 - V_{cc} = 1.8V to 5.5V
 - Full TTL compatible inputs and outputs
 - Auto increment for efficient data dump
- User Configured Memory Organization
 - By 16-bit or by 8-bit
- Hardware and software write protection
 - Defaults to write-disabled state at power-up
 - Software instructions for write-enable/disable
- Enhanced low voltage CMOS E²PROM technology
- Versatile, easy-to-use Interface
 - Self-timed programming cycle
 - Automatic erase-before-write
 - Programming status indicator
 - Word and chip erasable
 - Chip select enables power savings
- Durable and reliable
 - 40-year data retention after 1M write cycles
 - 1 million write cycles
 - Unlimited read cycles
 - Schmitt-trigger inputs
- Lead-free available

DESCRIPTION

The IS93C46D is a 1Kb non-volatile, ISSI® serial EEPROM. It is fabricated using an enhanced CMOS design and process. The IS93C46D contains power-efficient read/write memory, and organization of 128 bytes of 8 bits or 64 words of 16 bits. When the ORG pin is connected to V_{cc} or left unconnected, x16 is selected; when it is connected to ground, x8 is selected.

An instruction set defines the operation of the devices, including read, write, and mode-enable functions. To protect against inadvertent data modification, all erase and write instructions are accepted only while the device is write-enabled. A selected x8 byte or x16 word can be modified with a single WRITE or ERASE instruction. Additionally, the two instructions WRITE ALL or ERASE ALL can program the entire array. Once a device begins its self-timed program procedure, the data out pin (Dout) can indicate the READY/BUSY status by raising chip select (CS). The self-timed write cycle includes an automatic erase-before-write capability. The device can output any number of consecutive bytes/words using a single READ instruction.

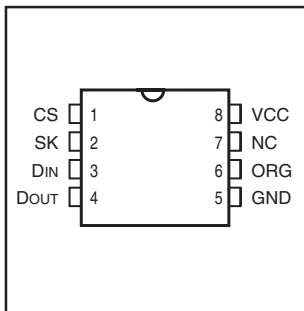
FUNCTIONAL BLOCK DIAGRAM



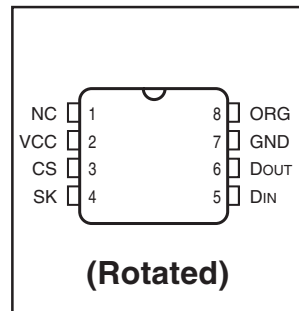
Copyright © 2005 Integrated Silicon Solution, Inc. All rights reserved. ISSI reserves the right to make changes to this specification and its products at any time without notice. ISSI assumes no liability arising out of the application or use of any information, products or services described herein. Customers are advised to obtain the latest version of this device specification before relying on any published information and before placing orders for products.

PIN CONFIGURATIONS

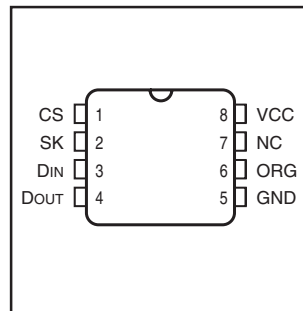
8-Pin DIP, 8-Pin TSSOP



8-Pin JEDEC SOIC "G"



8-Pin JEDEC SOIC "GR"



PIN DESCRIPTIONS

CS	Chip Select
SK	Serial Data Clock
DIN	Serial Data Input
DOUT	Serial Data Output
ORG	Organization Select
NC	Not Connected
Vcc	Power
GND	Ground

Applications

The IS93C46D is very popular in many applications which require low-power, low-density storage. Applications using this device include industrial controls, networking, and numerous other consumer electronics.

Endurance and Data Retention

The IS93C46D is designed for applications requiring up to 1M programming cycles (WRITE, WRALL, ERASE and ERAL). It provides 40 years of secure data retention without power after the execution of 1M programming cycles.

Device Operations

The IS93C46D is controlled by a set of instructions which are clocked-in serially on the Din pin. Before each low-to-high transition of the clock (SK), the CS pin must have already been raised to HIGH, and the Din value must be stable at either LOW or HIGH. Each

instruction begins with a start bit of the logical "1" or HIGH. Following this are the opcode (2 bits), address field (6 or 7 bits), and data, if appropriate. The clock signal may be held stable at any moment to suspend the device at its last state, allowing clock-speed flexibility. Upon completion of bus communication, CS would be pulled LOW. The device then would enter Standby mode if no internal programming is underway.

Read (READ)

The READ instruction is the only instruction that outputs serial data on the DOUT pin. After the read instruction and address have been decoded, data is transferred from the selected memory register into a serial shift register. (Please note that one logical "0" bit precedes the actual 8 or 16-bit output data string.) The output on DOUT changes during the low-to-high transitions of SK (see Figure 3).

Low Voltage Read

The IS93C46D has been designed to ensure that data read operations are reliable in low voltage environments. They provide accurate operation with Vcc as low as 1.8V.

Auto Increment Read Operations

In the interest of memory transfer operation applications, the IS93C46D has been designed to output a continuous stream of memory content in response to a single read operation instruction. To utilize this function, the system asserts a read instruction specifying a start location address. Once the 8 or 16 bits of the addressed register have been clocked out, the data in consecutively higher address locations is output. The address will wrap around continuously with CS HIGH until the chip select (CS) control pin is brought LOW. This allows for single instruction data dumps to be executed with a minimum of firmware overhead.

Write Enable (WEN)

The write enable (WEN) instruction must be executed before any device programming (WRITE, WRALL, ERASE, and ERAL) can be done. When Vcc is applied, this device powers up in the write disabled state. The device then remains in a write disabled state until a WEN instruction is executed. Thereafter, the device remains enabled until a WDS instruction is executed or until Vcc is removed. (See Figure 4.) (Note: Chip select must remain LOW until Vcc reaches its operational value.)

Write (WRITE)

The WRITE instruction includes 8 or 16 bits of data to be written into the specified register. After the last data bit has been applied to D_{IN}, and before the next rising edge of SK, CS must be brought LOW. If the device is write-enabled, then the falling edge of CS initiates the self-timed programming cycle (see WEN).

If CS is brought HIGH, after a minimum wait of 200 ns (5V operation) after the falling edge of CS (t_{CS}) D_{OUT} will indicate the READY/**BUSY** status of the chip. Logical “0” means programming is still in progress; logical “1” means the selected register has been written, and the part is ready for another instruction (see Figure 5). The READY/**BUSY** status will not be available if: a) The CS input goes HIGH after the end of the self-timed programming cycle, t_{WP}; or b) Simultaneously CS is HIGH, Din is HIGH, and SK goes HIGH, which clears the status flag.

Write All (WRALL)

The write all (WRALL) instruction programs all registers with the data pattern specified in the instruction. As with the WRITE instruction, the falling edge of CS must occur to initiate the self-timed programming cycle. If CS is then brought HIGH after a minimum wait of 200 ns (t_{CS}), the D_{OUT} pin indicates the READY/**BUSY** status of the chip (see Figure 6). Vcc is required to be above 4.5V for WRALL to function properly.

Write Disable (WDS)

The write disable (WDS) instruction disables all programming capabilities. This protects the entire device against accidental modification of data until a WEN instruction is executed. (When Vcc is applied, this part powers up in the write disabled state.) To protect data, a WDS instruction should be executed upon completion of each programming operation.

Erase Register (ERASE)

After the erase instruction is entered, CS must be brought LOW. The falling edge of CS initiates the self-timed internal programming cycle. Bringing CS HIGH after a minimum of t_{CS}, will cause D_{OUT} to indicate the READ/**BUSY** status of the chip: a logical “0” indicates programming is still in progress; a logical “1” indicates the erase cycle is complete and the part is ready for another instruction (see Figure 8).

Erase All (ERAL)

Full chip erase is provided for ease of programming. Erasing the entire chip involves setting all bits in the entire memory array to a logical “1” (see Figure 9). Vcc is required to be above 4.5V for ERAL to function properly.

INSTRUCTION SET - IS93C46D (1Kb)

Instruction ⁽²⁾	Start Bit	OP Code	8-bit Organization (ORG = GND)		16-bit Organization (ORG = Vcc)	
			Address ⁽¹⁾	Input Data	Address ⁽¹⁾	Input Data
READ	1	10	(A6-A0)	—	(A5-A0)	—
WEN (Write Enable)	1	00	11xxxxx	—	11xxxx	—
WRITE	1	01	(A6-A0)	(D7-D0)	(A5-A0)	(D15-D0)
WRALL (Write All Registers)	1	00	01xxxxx	(D7-D0)	01xxxx	(D15-D0)
WDS (Write Disable)	1	00	00xxxxx	—	00xxxx	—
ERASE	1	11	(A6-A0)	—	(A5-A0)	—
ERAL (Erase All Registers)	1	00	10xxxxx	—	10xxxx	—

Notes:

- x = Don't care bit.
- If the number of bits clocked-in does not match the number corresponding to a selected command, all extra trailing bits are ignored, and WRITE, WRALL, ERASE, ERAL are also ignored, and READ, WEN, WDS are accepted.

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Symbol	Parameter	Value	Unit
V _S	Supply Voltage	-0.5 to +6.5	V
V _P	Voltage on Any Pin	-0.5 to V _{CC} + 0.5	V
T _{BIAS}	Temperature Under Bias	-55 to +125	°C
T _{STG}	Storage Temperature	-65 to +150	°C
I _{OUT}	Output Current	5	mA

Notes:

1. Stress greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

OPERATING RANGE

Range	Ambient Temperature	V _{CC}
Industrial	-40°C to +85°C	1.8V to 5.5V
Automotive	-40°C to +125°C	2.5V to 5.5V

Note: ISSI offers Industrial grade for Commercial applications (0°C to +70°C)

CAPACITANCE

Symbol	Parameter	Conditions	Max.	Unit
C _{IN}	Input Capacitance	V _{IN} = 0V	5	pF
C _{OUT}	Output Capacitance	V _{OUT} = 0V	5	pF

DC ELECTRICAL CHARACTERISTICS

T_A = -40°C to +85°C for Industrial and -40°C to +125°C for Automotive.

Symbol	Parameter	Test Conditions	V _{CC}	Min.	Max.	Unit
V _{OL2}	Output LOW Voltage	I _{OL} = 100 μA	1.8V to 2.7V	—	0.2	V
V _{OL1}	Output LOW Voltage	I _{OL} = 2.1mA	2.7V to 5.5V	—	0.4	V
V _{OH2}	Output HIGH Voltage	I _{OH} = -100 μA	1.8V to 2.7V	V _{CC} - 0.2	—	V
V _{OH1}	Output HIGH Voltage	I _{OH} = -400 μA	2.7V to 5.5V	2.4	—	V
V _{IH}	Input HIGH Voltage		1.8V to 2.7V 2.7V to 5.5V	0.7xV _{CC} 2.0	V _{CC} +1 V _{CC} +1	V
V _{IL}	Input LOW Voltage		1.8V to 2.7V 2.7V to 5.5V	-0.3 -0.3	0.2xV _{CC} 0.8	V
I _{LI}	Input Leakage	V _{IN} = 0V to V _{CC} (CS, SK, D _{IN} , ORG)		0	2.5	μA
I _{LO}	Output Leakage	V _{OUT} = 0V to V _{CC} , CS = 0V		0	2.5	μA

Notes:

Automotive grade devices in this table are tested with V_{CC} = 2.5V to 5.5V and 4.5V to 5.5V. An operation with V_{CC} < 2.5V is not specified.

POWER SUPPLY CHARACTERISTICS

T_A = -40°C to +85°C for Industrial, -40°C to +125°C for Automotive.

Symbol	Parameter	Test Conditions	V _{CC}	Min.	Typ.	Max.	Unit
I _{CC1}	V _{CC} Read Supply Current	CS = V _{IH} , SK = 1 MHz, CMOS input levels	1.8V	—	0.1	1	mA
		CS = V _{IH} , SK = 2 MHz, CMOS input levels	2.5V	—	0.2	1	mA
		CS = V _{IH} , SK = 2 MHz, CMOS input levels	5.0V	—	0.5	2	mA
I _{CC2}	V _{CC} Write Supply Current	CS = V _{IH} , SK = 1 MHz, CMOS input levels	1.8V	—	0.5	1	mA
		CS = V _{IH} , SK = 2 MHz, CMOS input levels	2.5V	—	1	2	mA
		CS = V _{IH} , SK = 2 MHz, CMOS input levels	5.0V	—	2	3	mA
I _{SB1}	Standby Current	CS = GND, SK = GND	1.8V	—	0.1	1	μA
		ORG = V _{CC} or Floating (x16)	2.5V	—	0.1	2	μA
		D _{IN} = V _{CC} or GND	5.0V	—	0.2	4	μA
I _{SB2}	Standby Current	CS = GND, SK = GND	1.8V	—	6	10	μA
		ORG = GND (x8)	2.5V	—	6	10	μA
		D _{IN} = V _{CC} or GND	5.0V	—	10	15	μA

AC ELECTRICAL CHARACTERISTICS

TA = -40°C to +85°C for Industrial

Symbol	Parameter	Test Conditions	Min.	Max.	Unit	
f _{SK}	SK Clock Frequency	1.8V ≤ V _{CC} < 2.5V	0	1	Mhz	
		2.5V ≤ V _{CC} < 4.5V	0	2	Mhz	
		4.5V ≤ V _{CC} ≤ 5.5V	0	3	Mhz	
t _{SKH}	SK HIGH Time	1.8V ≤ V _{CC} < 2.5V	250	—	ns	
		2.5V ≤ V _{CC} < 4.5V	200	—	ns	
		4.5V ≤ V _{CC} ≤ 5.5V	200	—	ns	
t _{SKL}	SK LOW Time	1.8V ≤ V _{CC} < 2.5V	250	—	ns	
		2.5V ≤ V _{CC} < 4.5V	200	—	ns	
		4.5V ≤ V _{CC} ≤ 5.5V	100	—	ns	
t _{CS}	Minimum CS LOW Time	1.8V ≤ V _{CC} < 2.5V	250	—	ns	
		2.5V ≤ V _{CC} < 4.5V	200	—	ns	
		4.5V ≤ V _{CC} ≤ 5.5V	200	—	ns	
t _{CSS}	CS Setup Time	Relative to SK	1.8V ≤ V _{CC} < 2.5V	200	—	ns
		2.5V ≤ V _{CC} < 4.5V	100	—	ns	
		4.5V ≤ V _{CC} ≤ 5.5V	50	—	ns	
t _{DIS}	Din Setup Time	Relative to SK	1.8V ≤ V _{CC} < 2.5V	100	—	ns
		2.5V ≤ V _{CC} < 4.5V	50	—	ns	
		4.5V ≤ V _{CC} ≤ 5.5V	50	—	ns	
t _{CSH}	CS Hold Time	Relative to SK	1.8V ≤ V _{CC} < 2.5V	0	—	ns
		2.5V ≤ V _{CC} < 4.5V	0	—	ns	
		4.5V ≤ V _{CC} ≤ 5.5V	0	—	ns	
t _{DIH}	Din Hold Time	Relative to SK	1.8V ≤ V _{CC} < 2.5V	50	—	ns
		2.5V ≤ V _{CC} < 4.5V	50	—	ns	
		4.5V ≤ V _{CC} ≤ 5.5V	50	—	ns	
t _{PD1}	Output Delay to "1"	AC Test	1.8V ≤ V _{CC} < 2.5V	—	400	ns
		2.5V ≤ V _{CC} < 4.5V	—	200	ns	
		4.5V ≤ V _{CC} ≤ 5.5V	—	100	ns	
t _{PD0}	Output Delay to "0"	AC Test	1.8V ≤ V _{CC} < 2.5V	—	400	ns
		2.5V ≤ V _{CC} < 4.5V	—	200	ns	
		4.5V ≤ V _{CC} ≤ 5.5V	—	100	ns	
t _{SV}	CS to Status Valid	AC Test	1.8V ≤ V _{CC} < 2.5V	—	400	ns
		2.5V ≤ V _{CC} < 4.5V	—	200	ns	
		4.5V ≤ V _{CC} ≤ 5.5V	—	200	ns	
t _{DF}	CS to Dout in 3-state	AC Test, CS=VIL	1.8V ≤ V _{CC} < 2.5V	—	100	ns
		2.5V ≤ V _{CC} < 4.5V	—	100	ns	
		4.5V ≤ V _{CC} ≤ 5.5V	—	100	ns	
t _{WP}	Write Cycle Time	1.8V ≤ V _{CC} < 2.5V	—	10	ms	
		2.5V ≤ V _{CC} < 4.5V	—	5	ms	
		4.5V ≤ V _{CC} ≤ 5.5V	—	5	ms	

Notes:

1. C_L = 100pF

AC ELECTRICAL CHARACTERISTICS

TA = -40°C to +125°C for Automotive

Symbol	Parameter	Test Conditions	Min.	Max.	Unit	
f _{SK}	SK Clock Frequency	2.5V ≤ V _{CC} < 4.5V	0	2	Mhz	
		4.5V ≤ V _{CC} ≤ 5.5V	0	3	Mhz	
t _{SKH}	SK HIGH Time	2.5V ≤ V _{CC} < 4.5V	200	—	ns	
		4.5V ≤ V _{CC} ≤ 5.5V	200	—	ns	
t _{SKL}	SK LOW Time	2.5V ≤ V _{CC} < 4.5V	200	—	ns	
		4.5V ≤ V _{CC} ≤ 5.5V	100	—	ns	
t _{CS}	Minimum CS LOW Time	2.5V ≤ V _{CC} < 4.5V	200	—	ns	
		4.5V ≤ V _{CC} ≤ 5.5V	200	—	ns	
t _{CS} S	CS Setup Time	Relative to SK	2.5V ≤ V _{CC} < 4.5V	100	—	ns
		4.5V ≤ V _{CC} ≤ 5.5V	50	—	ns	
t _{DIS}	Din Setup Time	Relative to SK	2.5V ≤ V _{CC} < 4.5V	50	—	ns
		4.5V ≤ V _{CC} ≤ 5.5V	50	—	ns	
t _{CSH}	CS Hold Time	Relative to SK	2.5V ≤ V _{CC} < 4.5V	0	—	ns
		4.5V ≤ V _{CC} ≤ 5.5V	0	—	ns	
t _{DIH}	Din Hold Time	Relative to SK	2.5V ≤ V _{CC} < 4.5V	50	—	ns
		4.5V ≤ V _{CC} ≤ 5.5V	50	—	ns	
t _{PD1}	Output Delay to "1"	AC Test	2.5V ≤ V _{CC} < 4.5V	—	200	ns
		4.5V ≤ V _{CC} ≤ 5.5V	—	100	ns	
t _{PD0}	Output Delay to "0"	AC Test	2.5V ≤ V _{CC} < 4.5V	—	200	ns
		4.5V ≤ V _{CC} ≤ 5.5V	—	100	ns	
t _{SV}	CS to Status Valid	AC Test	2.5V ≤ V _{CC} < 4.5V	—	200	ns
		4.5V ≤ V _{CC} ≤ 5.5V	—	200	ns	
t _{DF}	CS to Dout in 3-state	AC Test, CS=VIL	2.5V ≤ V _{CC} < 4.5V	—	100	ns
		4.5V ≤ V _{CC} ≤ 5.5V	—	100	ns	
t _{WP}	Write Cycle Time	2.5V ≤ V _{CC} < 4.5V	—	5	ms	
		4.5V ≤ V _{CC} ≤ 5.5V	—	5	ms	

Notes:

1. C_L = 100pF

AC WAVEFORMS

FIGURE 2. SYNCHRONOUS DATA TIMING

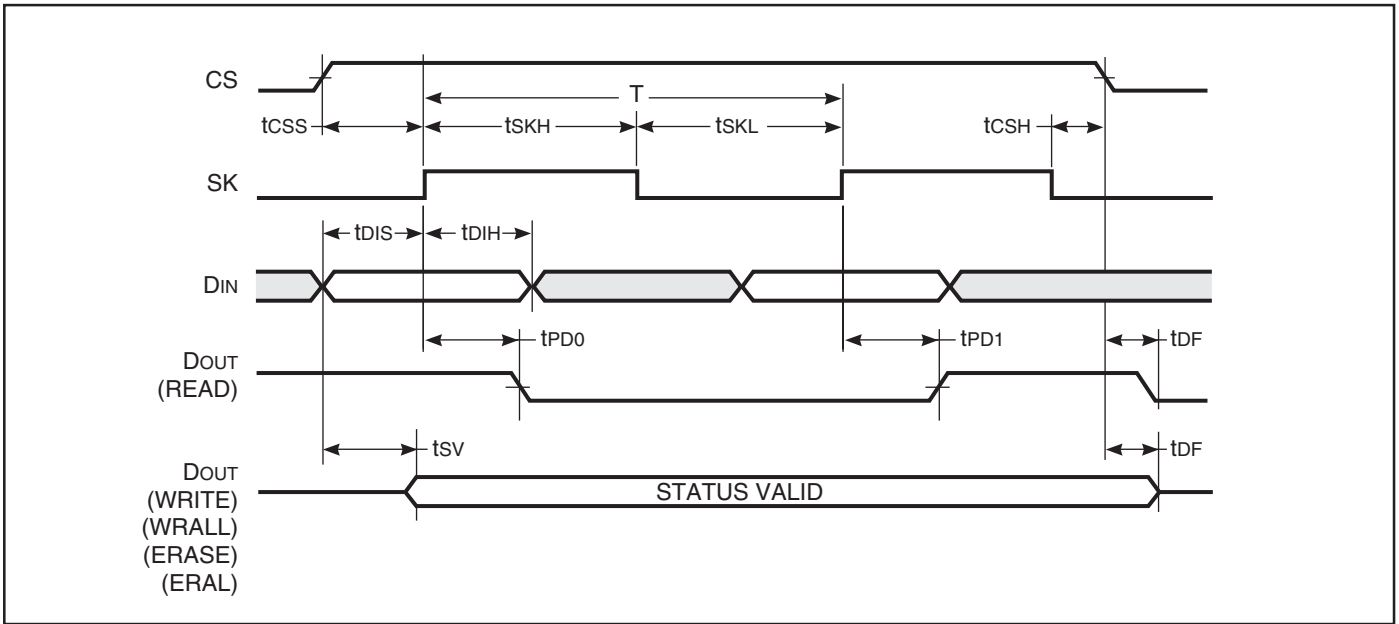
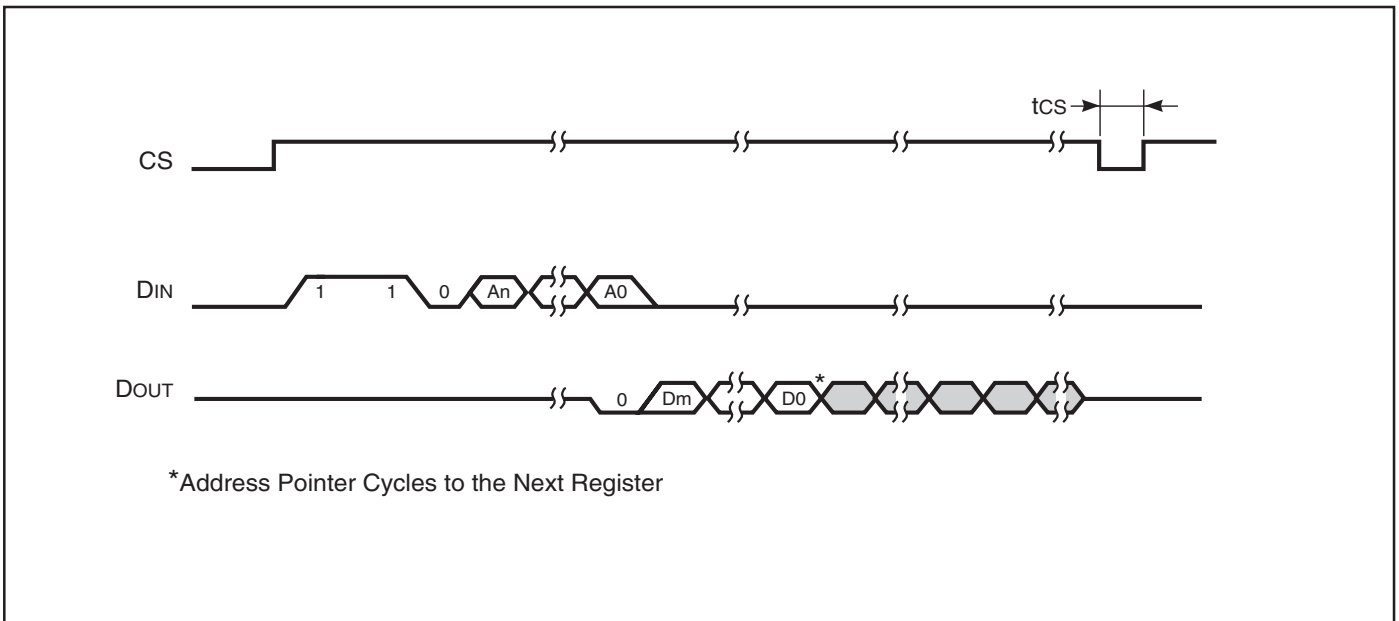


FIGURE 3. READ CYCLE TIMING



Notes:

To determine address bits A_n - A_0 and data bits D_m - D_0 , see Instruction Set for the specific device.

AC WAVEFORMS

FIGURE 4. WRITE ENABLE (WEN) CYCLE TIMING

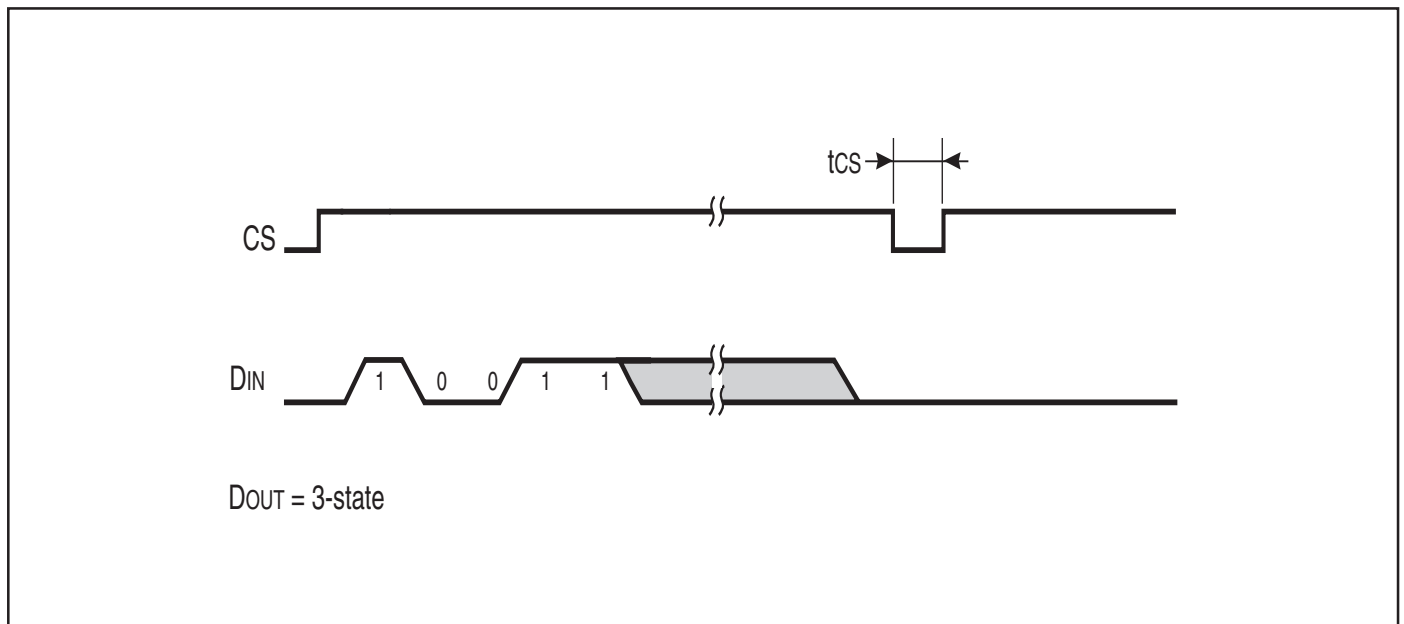
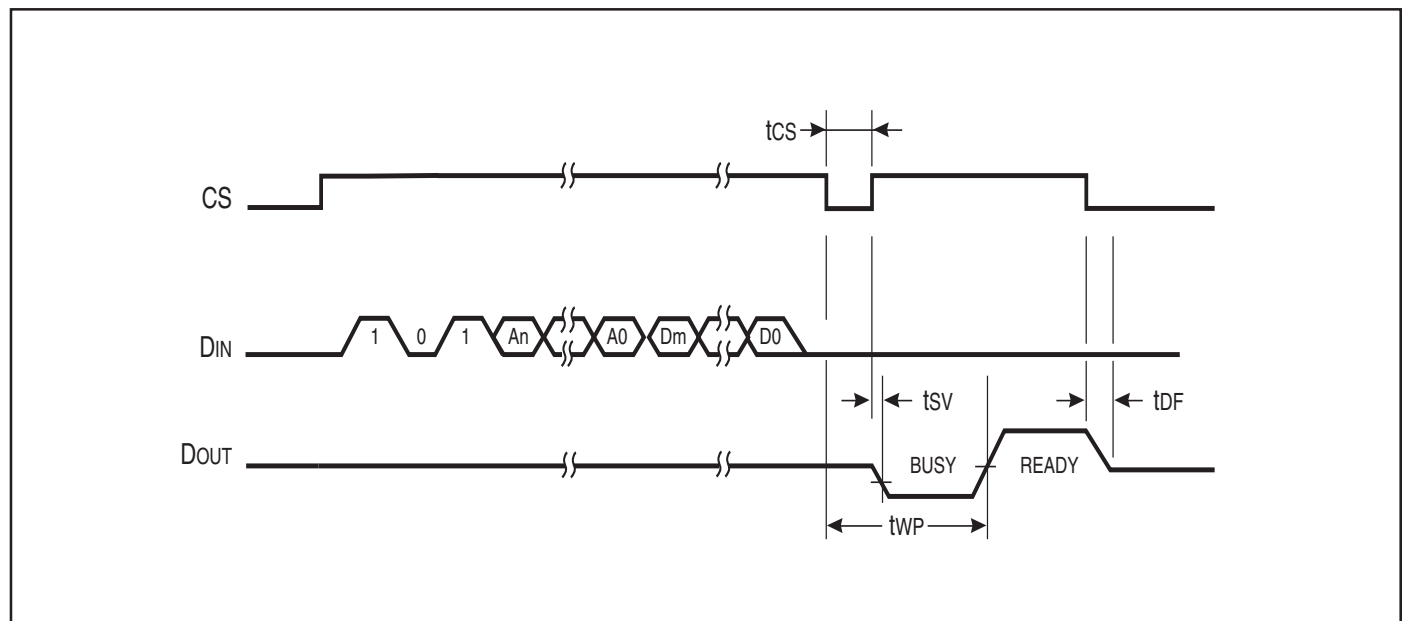


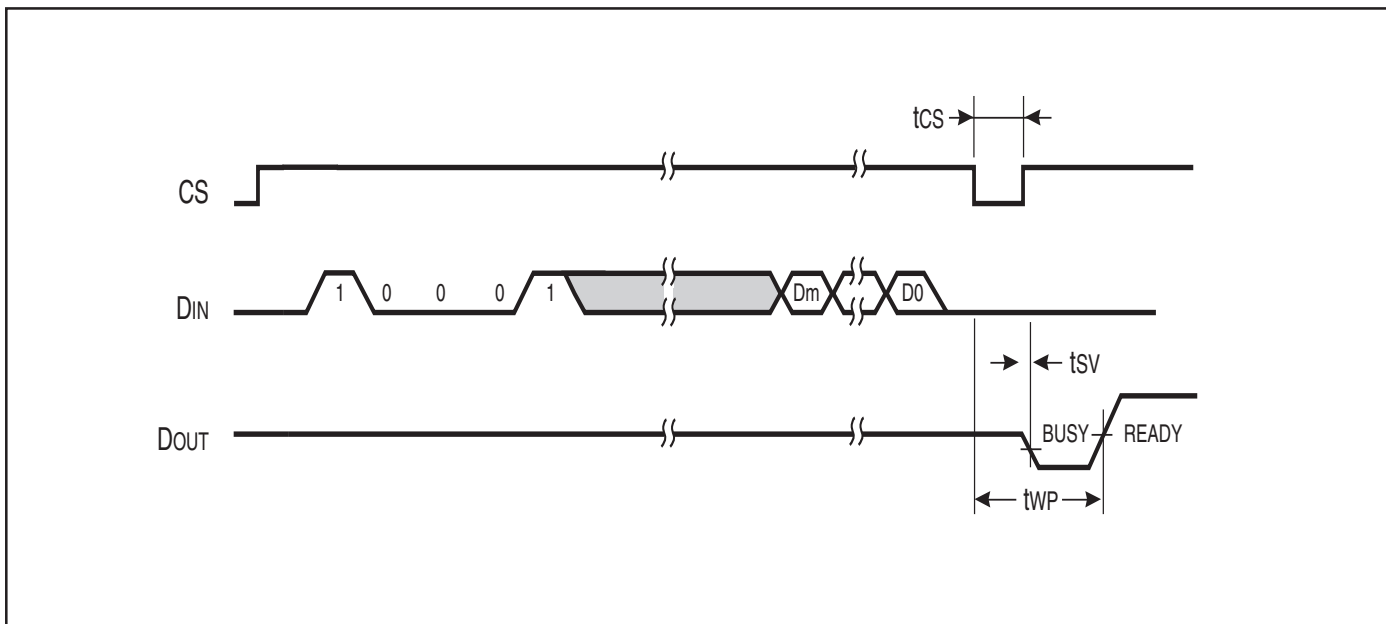
FIGURE 5. WRITE (WRITE) CYCLE TIMING

**Notes:**

1. After the completion of the instruction (Dout is in READY status) then it may perform another instruction. If device is in **BUSY** status (Dout indicates **BUSY** status) then attempting to perform another instruction could cause device malfunction.
2. To determine address bits A_n - A_0 and data bits D_m - D_0 , see Instruction Set for the specific device.

AC WAVEFORMS

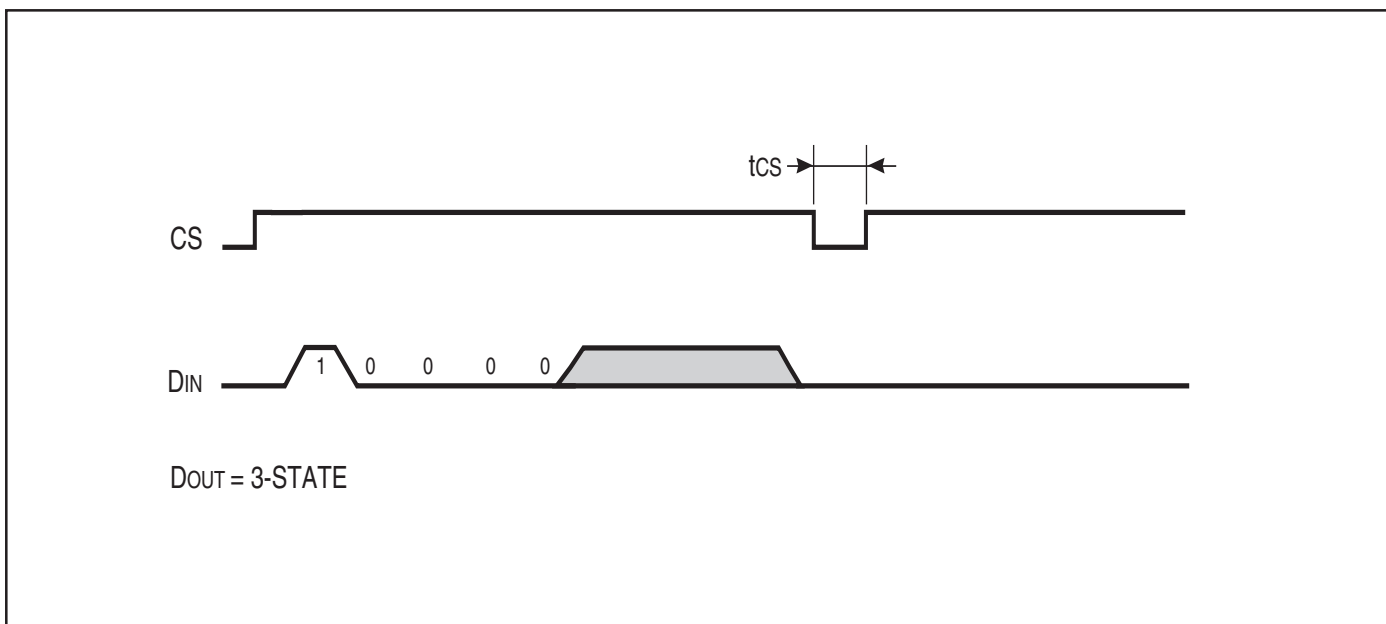
FIGURE 6. WRITE ALL (WRALL) CYCLE TIMING



Notes:

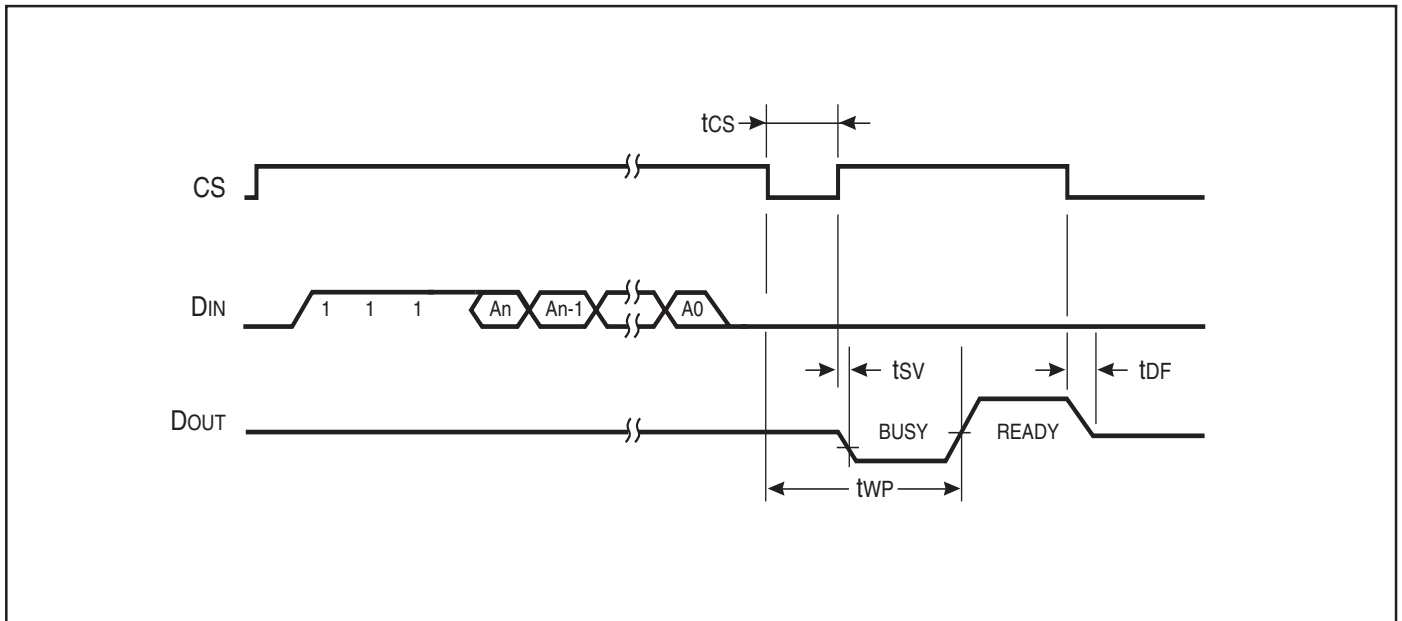
1. After the completion of the instruction (DOUT is in READY status) then it may perform another instruction. If device is in **BUSY** status (DOUT indicates **BUSY** status) then attempting to perform another instruction could cause device malfunction.
2. To determine data bits D_m - D_0 , see Instruction Set for the appropriate device.

FIGURE 7. WRITE DISABLE (WDS) CYCLE TIMING



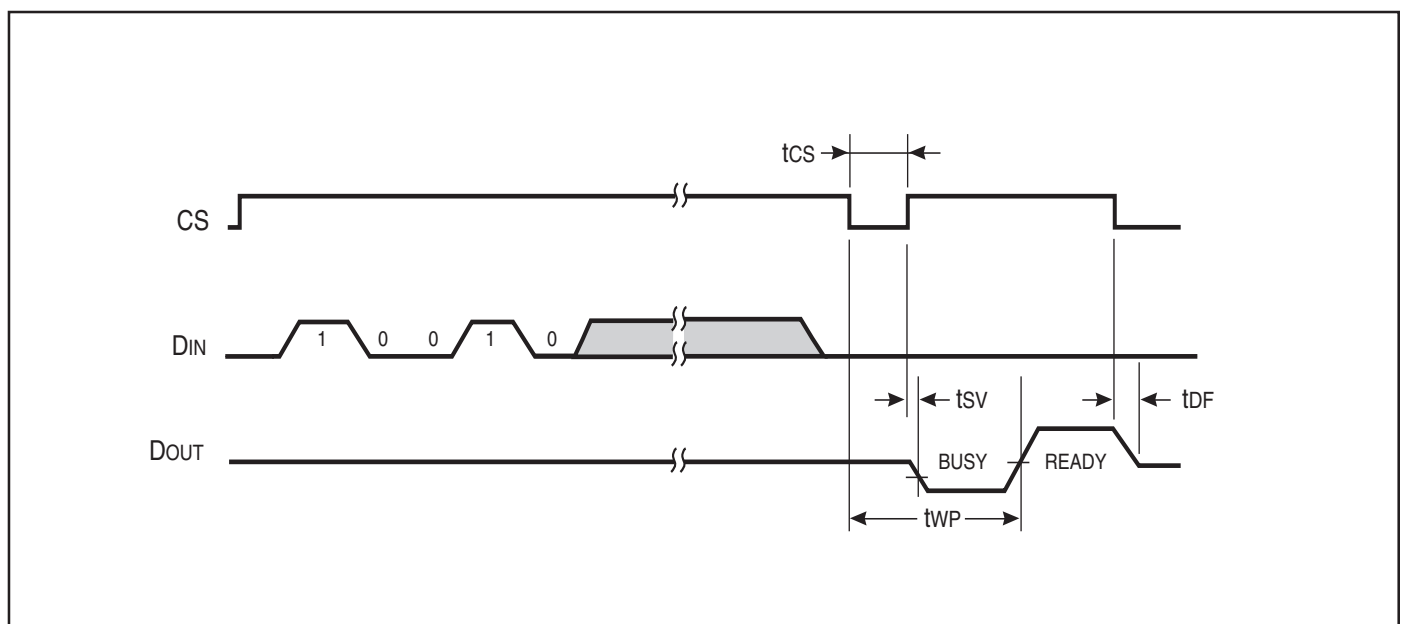
AC WAVEFORMS

FIGURE 8. ERASE (REGISTER ERASE) CYCLE TIMING

**Notes:**

To determine data bits An - A0, see Instruction Set for the appropriate device.

FIGURE 9. ERASE ALL (ERAL) CYCLE TIMING

**Note for Figures 8 and 9:**

After the completion of the instruction (DOUT is in READY status) then it may perform another instruction. If device is in **BUSY** status (DOUT indicates **BUSY** status) then attempting to perform another instruction could cause device malfunction.

ORDERING INFORMATION**Industrial Range: -40°C to +85°C**

Voltage Range	Order Part No.	Package
1.8V to 5.5V	IS93C46D-2PI	300-mil Plastic DIP
	IS93C46D-2GI	SOIC (rotated) JEDEC
	IS93C46D-2GRI	SOIC JEDEC
	IS93C46D-2ZI	169-mil TSSOP

ORDERING INFORMATION**Industrial Range: -40°C to +85°C, Lead-free**

Voltage Range	Order Part No.	Package
1.8V to 5.5V	IS93C46D-2PLI	300-mil Plastic DIP
	IS93C46D-2GLI	SOIC (rotated) JEDEC
	IS93C46D-2GRLI	SOIC JEDEC
	IS93C46D-2ZLI	169-mil TSSOP

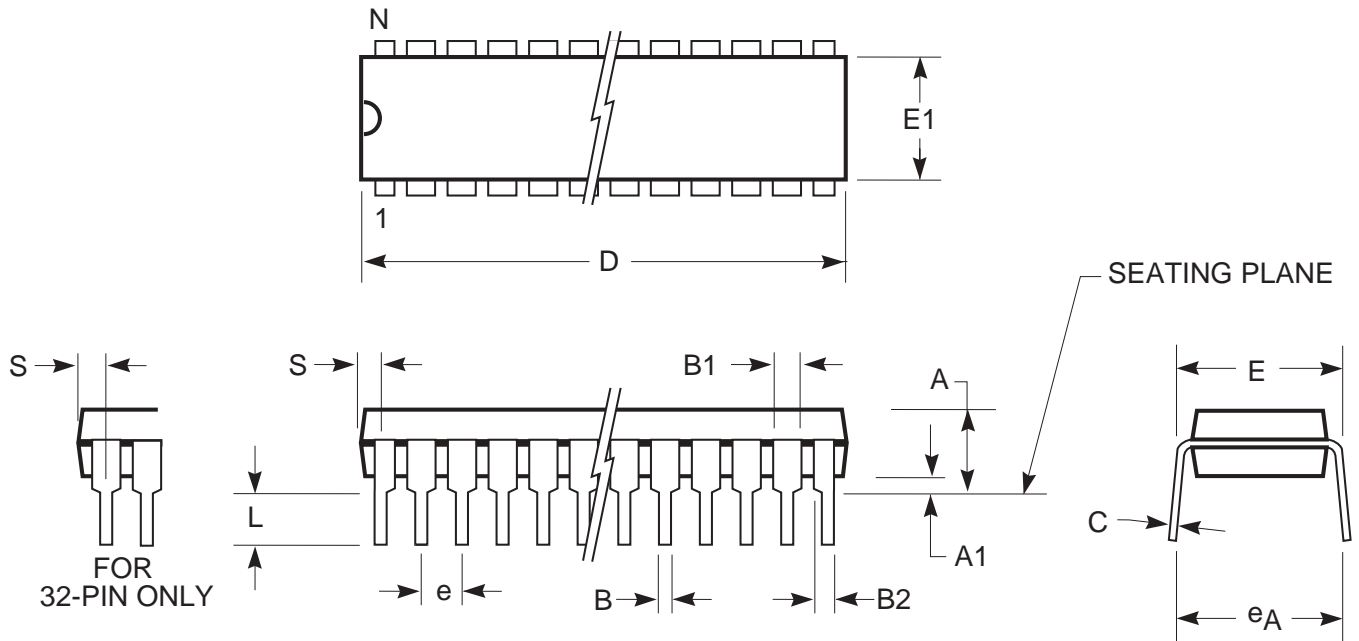
ORDERING INFORMATION**Automotive Range: -40°C to +125°C, Lead-free**

Voltage Range	Order Part No.	Package
2.5V to 5.5V	IS93C46D-3PLA3	300-mil Plastic DIP
	IS93C46D-3GRLA3	SOIC JEDEC

PACKAGING INFORMATION



300-mil Plastic DIP
Package Code: N,P



Sym.	MILLIMETERS		INCHES	
	Min.	Max.	Min.	Max.
NO. Leads	8			
A	3.68	4.57	0.145	0.180
A1	0.38	—	0.015	—
B	0.36	0.56	0.014	0.022
B1	1.14	1.52	0.045	0.060
B2	0.81	1.17	0.032	0.046
C	0.20	0.33	0.008	0.013
D	9.12	9.53	0.359	0.375
E	7.62	8.26	0.300	0.325
E1	6.20	6.60	0.244	0.260
eA	8.13	9.65	0.320	0.380
e	2.54 BSC		0.100 BSC	
L	3.18	—	0.125	—
S	0.64	0.762	0.025	0.030

Notes:

1. Controlling dimension: inches, unless otherwise specified.
2. BSC = Basic lead spacing between centers.
3. Dimensions D and E1 do not include mold flash protrusions and should be measured from the bottom of the package.
4. Formed leads shall be planar with respect to one another within 0.004 inches at the seating plane.

Copyright © 2003 Integrated Silicon Solution, Inc. All rights reserved. ISSI reserves the right to make changes to this specification and its products at any time without notice. ISSI assumes no liability arising out of the application or use of any information, products or services described herein. Customers are advised to obtain the latest version of this device specification before relying on any published information and before placing orders for products.

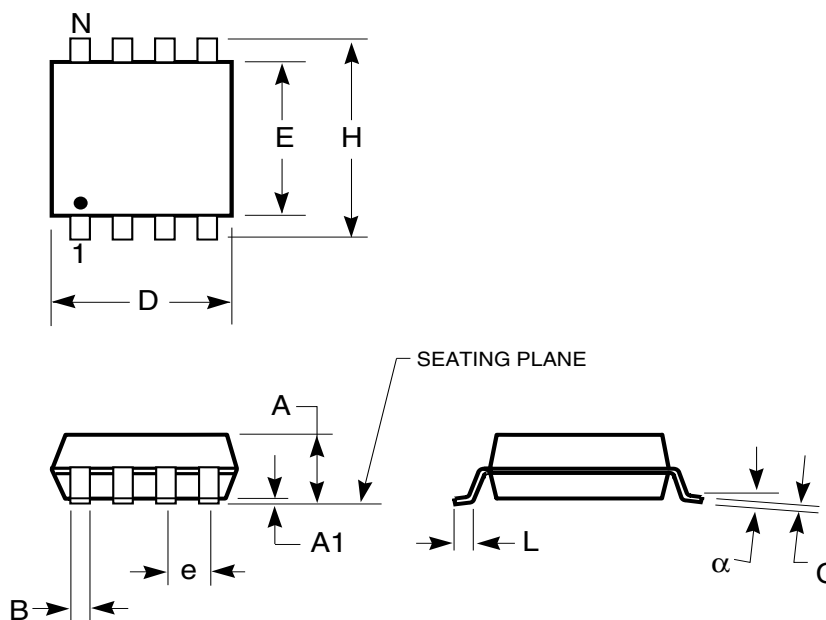
Integrated Silicon Solution, Inc. — www.issi.com — 1-800-379-4774

Rev. D
 02/14/03

PACKAGING INFORMATION



150-mil Plastic SOP
 Package Code: G, GR



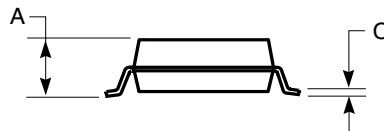
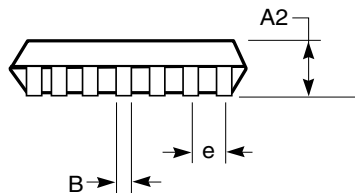
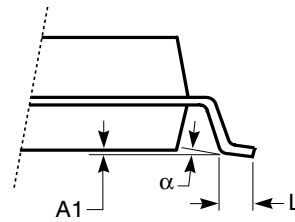
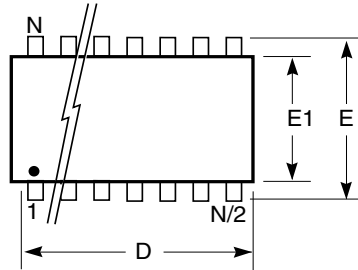
150-mil Plastic SOP (G, GR)				
Symbol	Min	Max	Min	Max
Ref. Std.	Inches		mm	
No. Leads	8		8	
A	—	0.068	—	1.73
A1	0.004	0.009	0.1	0.23
B	0.013	0.020	0.33	0.51
C	0.007	0.010	0.18	0.25
D	0.189	0.197	4.8	5
E	0.150	0.157	3.81	3.99
H	0.228	0.245	5.79	6.22
e	0.050 BSC		1.27 BSC	
L	0.020	0.035	0.51	0.89

Notes:

1. Controlling dimension: inches, unless otherwise specified.
2. BSC = Basic lead spacing between centers.
3. Dimensions D and E1 do not include mold flash protrusions and should be measured from the bottom of the package.
4. Formed leads shall be planar with respect to one another within 0.004 inches at the seating plane.

PACKAGING INFORMATION

Thin Shrink Small Outline TSSOP
 Package Code: Z (8 pin, 14 pin)



TSSOP (Z)				
Ref. Std.	JEDEC MO-153			
No. Leads	8			
	Millimeters		Inches	
Symbol	Min	Max	Min	Max
A	—	1.20	—	0.047
A1	0.05	0.15	0.002	0.006
A2	0.80	1.05	0.032	0.041
B	0.19	0.30	0.007	0.012
C	0.09	0.20	0.004	0.008
D	2.90	3.10	0.114	0.122
E1	4.30	4.50	0.169	0.177
E	6.40 BSC		0.252 BSC	
e	0.65 BSC		0.026 BSC	
L	0.45	0.75	0.018	0.030
alpha	—	8°	—	8°

TSSOP (Z)				
Ref. Std.	JEDEC MO-153			
No. Leads	14			
	Millimeters		Inches	
Symbol	Min	Max	Min	Max
A	—	1.20	—	0.047
A1	0.05	0.15	0.002	0.006
A2	0.80	1.05	0.031	0.041
B	0.19	0.30	0.007	0.012
C	0.09	0.20	0.0035	0.008
D	4.90	5.10	0.193	0.201
E1	4.30	4.50	0.170	0.177
E	6.40 BSC		0.252 BSC	
e	0.65 BSC		0.026 BSC	
L	0.45	0.75	0.0177	0.0295
alpha	—	8°	—	8°

ISSI reserves the right to make changes to its products at any time without notice in order to improve design and supply the best possible product. We assume no responsibility for any errors which may appear in this publication. © Copyright 2002, Integrated Silicon Solution, Inc.